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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,310	11/23/2004	Roman Woyzichovski	10901/81	6114

26646 7590 08/18/2009
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ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
08/18/2009	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/501,310
Filing Date: November 23, 2004
Appellant(s): WOYZICHOVSKI, ROMAN

Clifford A. Ulrich
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 4, 2009 appealing from the Office action mailed September 5, 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

U.S. Pat. No. 5079549 to Liessner; 1-1992

U.S. Pat. No. 5134578 to Gaverick et al; 7-1992

U.S. Pub. No. 2002/0116181 to Khan et al; 8-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. <u>Claims 21-24, 26, 27, and 30-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner (U.S. Pat. No. 5079549 – previously cited) in view of Garverick et al (U.S. Pat. No. 5134578; "Garverick" – previously cited).</u>

Regarding claim 21, Liessner discloses a method for interpolating (col. 2, lines 20-25) at least two position-dependent, periodic analog signals (fig. 1, SIN(X), COS(X)) that are phase-shifted with respect to one another and which are generated by scanning a measuring scale (abstract), comprising: generating a string of results (fig. 1, "ERROR SIGNAL") by combining (fig. 1, ref. 20) the periodic analog signals with correctional values (fig. 1, outputs of 16 and 18) and subsequently combining the periodic analog signals with one another; generating from the string of results (a) new correctional values (new or updated outputs of fig. 1, refs. 16 and 18) in accordance in accordance with a quality criterion (fig. 1, output of error "DETECTOR"; "ES>0" or "ES<0") that is to be satisfied during interpolation (col. 3, lines 40-55) and (b) output signals of the interpolation (fig. 1, "Y"); accumulating (fig. 1, ref. 24; fig. 4A, refs. 25 and 27) over a specifiable time interval (according to disable pulse generator, i.e. fig. 4A, ref. 29) values

of the combination output for generating the correctional values (outputs of fig. 1, refs. 16 and 18) and output signals (fig. 1, “Y”); and using a signal sequence generated by the accumulation as an address sequence (also fig. 1, “Y”) for generating the correctional values and for generating the output signals (fig. 1). Liessner discloses that the multipliers or combiners (fig. 1, refs. 12 and 14) which combine the periodic analog signals (fig. 1, SIN(X), COS(X)) with correctional values (fig. 1, outputs of 16 and 18) are “multiplying digital to analog converters that cause a digital input to attenuate an analog signal” (col. 3, lines 25-30). Therefore, the outputs from the lookup tables (fig. 1, refs. 16 and 18) are digital and the periodic signals (fig. 1, SIN(X), COS(X)) are analog ones which are attenuated according to the outputs from the lookup tables. Liessner does not explicitly disclose using sigma-delta modulators to convert the periodic analog signals into digital signals. However, the use of digital data to represent analog waveforms is notoriously known in the art as evidenced by Garverick. The use of sigma-delta analog to digital converters is well known in the art as evidenced by Garverick. Garcerick discloses the use of several sigma-delta analog to digital converters (fig. 1, refs. 21-26) to convert various phases of an analog signal into digital form (col. 4, lines 14-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the Liessner’s "rotary or linear encoder” output (fig. 1, "SIN(X)" and "COS(X)") could be converted into digital form before being fed to multipliers (fig. 1, refs. 12 and 14) as suggested by Garverick. In the combination of Liessner in view of Garverick, Liessner’s embodiment must be converted to a purely digital one. One skilled in the art would be enabled to complete the conversion with knowledge readily known in the art and motivated to complete the conversion because of the advantages provided by digital implementations of analog devices. Namely,

proper digital implementations provide for zero loss in signal integrity as notoriously understood in the art.

Regarding claims 22 and 23, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, as broadly as claimed, Liessner's counter (fig. 1, ref. 24) is considered to be both a filter and an integrator because its output depends upon an accumulation of the past inputs.

Regarding claim 24, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses forming the address sequence (fig. 1, "Y") from the accumulation (fig. 1, ref. 24), the address sequence including address values that represent phase information of the analog signals (col. 3, lines 35-40).

Regarding claim 26, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address values are a linear function of the phases of the periodic signals when the quality criterion is satisfied. The address values are a linear function of the phases because the error of phases directly determine the address values in a linear fashion (col. 4, lines 19-38).

Regarding claim 27, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address sequence (fig. 1, "Y") represent a phase value having a fractional proportion (col. 3, lines 35-40).

Regarding claim 30, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the generation of new correctional values is in accordance with the quality criterion (amount of error) until it is satisfied because the embodiment is a closed loop embodiment (fig. 1).

Regarding claim 31, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses storing possible correction values as predefined values in an assignment unit (col. 3, lines 35-40).

Regarding claim 32, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied in claim 21 above.

Regarding claim 33, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the correctional values correspond to values of a trigonometric function (col. 3, lines 35-40).

Regarding claim 34, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are phase shifted by 90 degrees with respect to each other as applied in claim 21 above.

Regarding claim 35, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are substantially sinusoid as applied in claim 21 above.

Regarding claim 36, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to multiplying (fig. 1, refs. 12 and 14).

Regarding claim 37, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, it is inherent that a piece of data may have a word width of one bit as understood by one having ordinary skill in the art.

Regarding claim 38, Liessner in view of Garverick disclose the limitations of claim 36 as applied above. Further, Liessner discloses the remaining limitations of the claim

as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to reducing or attenuating (fig. 1, refs. 12 and 14; col. 3, lines 25-30; “attenuating”).

Regarding claim 39, Liessner in view of Garverick disclose the limitations of claim 38 as applied above. Further, Liessner discloses combining by addition (fig. 1, ref. 20) the correctional values. Furthermore, in the purely digital implementation of Liessner in view of Garverick, the addition of the correctional values would result in one of four possibilities as understood by one having ordinary skill in the art because no other possibilities could exist.

Regarding claim 40, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above.

Regarding claim 41, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above.

Regarding claim 42, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above. Liessner in view of Garverick do not explicitly disclose an evaluation circuit post-connected to the filter configured to convert address values of the address sequence into output values of the interpolation. However, Liessner discloses that “the digital output signal y is provided that *represents* displacement within a reticle cycle" (col. 2, lines 25-30). Because the digital output signal y only “represents” the displacement, it is obvious to one having ordinary skill in the art that an evaluation circuit would be required to convert the digital address value y into more useful information. Moreover, Liessner suggests that the evaluation circuit may be a memory lookup table such as references 16 or 18 of figure 1 (col. 3, lines 35-45). Therefore, it would have been obvious to one having ordinary skill in the art at the

time which the invention was made that an evaluation unit would be required to convert Liessner's y address values into a more useable format for their utility.

3. Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner in view of Garverick, and in further view of The Applicant's Admitted Prior Art ("AAPA").

Regarding claim 25, Liessner in view of Garverick disclose the limitations of claim 24 as applied above. Liessner does not explicitly disclose that the output signals (fig. 1, "Y") are generated from the address sequence by low- pass filtering and assignment of the address values. However, low-pass filtering and assignment of the address values is well known in the art as evidenced in the discussion of the AAPA (page 2, lines 7-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the address sequence of Liessner could be fed through a low-pass filter (i.e. within UP/DOWN counter 26 of figure 1) as suggested by the AAPA because it was a well known method in the art.

4. Claims 28 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner in view of Garverick, and Khan et al (U.S. Pat. Pub. 2002/0116181; hereafter "Khan" – newly cited).

Regarding claim 28, Liessner in view of Garverick disclose the limitations of claim 27 as applied above. Liessner in view of Garverick do not explicitly disclose that the correctional values are generated in the correctional value generating step in accordance with a high-value part and low-value part of the address sequence, the high-value part corresponding to an integer portion of the address values. However, Khan teaches an exemplary sine/cosine mapper according to figure 2 for determining from an upper two bits (input to 222) of the phase accumulation a quadrant in which a phase corresponding to the phase accumulation is located on an X-Y coordinate plane (para.

0055), a look-up table (226) for storing a predetermined number of sine or cosine values for one of four determined quadrants of the X-Y coordinate plane, and outputting a sine or cosine value (20 bits each "COS" and "SIN" output from 226) according to bits of the phase accumulation other than the upper two bits (i.e. “lower bits”; 18 remaining bits of 20 not fed into "OUTPUT SELECT" 222), and a cosine and sine value calculator (222) for calculating the sine and cosine values having phase corresponding to the phase accumulation according to the determined quadrant and the sine or cosine value received from the look-up table (paras. 0055-0058). Khan teaches the implementation of the mapper is effective and reduces overhead (para. 0010). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the sine/cosine lookup tables of Liessner (fig. 1, refs. 12 and 14) could be replaced by the implementation taught by Khan because it is an effective method which reduces overhead.

Regarding claim 29, Liessner in view of Garverick disclose the limitations of claim 27 as applied above. Further, Liessner in view of Garverick, and Khan disclose the remaining limitations of the claim as applied to claim 28 above.

(10) Response to Argument

The Applicant has presented the following arguments against the application of the prior art combination of Liessner (U.S. Pat. No. 5079549) in view of Garverick et al (U.S. Pat. No. 5134578; “Garverick”): (1) the combination does not support a fully digital implementation of the claimed invention and requires a substantial redesign of the primary reference Liessner and (2) Liessner does not disclose accumulating results for generating correctional values over a specifiable time interval.

Regarding the Applicant's argument (1), the Examiner argues that the combination of Liessner in view of Garverick would result in a fully functional digital implementation of *certain ones* of Liessner's original analog components. Specifically, by utilizing a sigma delta analog to digital converter (such as, for example, one of the ones from Gaverick's figure 1, refs. 21-26) to convert Liessner's rotary encoded outputs (fig. 1, output of ref. 10) into digital representations of such outputs, Liessner's multipliers (fig. 1, refs, 12 and 14) as well as Liessner's adder (fig. 1, ref. 20) would be replaced with ones that operate in a digital fashion.

Although the Applicant suggests that the Examiner's proposed combination of Liessner and Garverick would result in an inoperative or principal-changing "redesign" of Liessner's original invention, the Examiner insists that any and all changes required for an operative combination are well within the level of one having ordinary skill in the art and would only result in routine and predictable results. <u>The Examiner suggest that a proficient engineer working in the electrical arts would be able to design "mirror" analog or digital embodiments of the same circuit and would immediately be aware of the advantages and/or disadvantages of each.</u> In the combination as presented by the Examiner, Liessner's "basic principal" of operation would be maintained in a digital implementation as would be readily understood by one having ordinary skill in the art. As is notoriously known and understood in the art, properly designed digital implementations provide for zero loss in signal integrity. Moreover, the Applicant's assertion that every component of Liessner's invention would have to be modified to

accommodate the combination is untrue. The Applicant notes that Liessner's output signal "ES" is an analog one (appeal brief, pg. 6, line 22). The Examiner agrees and notes that, in the proposed combination, it could remain as an analog signal. That is, the analog functions of Liessner's circuit components 22, 23, 24, and 26 in figure 1 could remain as they are presently configured. Only Liessner's multipliers (12 and 14) and adder (20) would be modified to digital form for advantages of the combination to be achieved (i.e., the adder 20 could add digital values and output an analog output in return). As already stated, the principal advantage would be to achieve zero loss in accuracy. Other advantages are commonly known to one having ordinary skill in the art and should likewise be considered. Finally, the Examiner notes that the Applicant has not provided, in the specification or otherwise, any peculiar features, synergy, unexpected result, or other indicia of non-obviousness in the use of sigma delta analog to digital converters in the claimed invention.

Regarding the Applicant's argument (2), the accumulation of UP and DOWN outputs (via fig. 4A, refs. 25 and 27) from Liessner's error signal detector (fig. 4A, ref. 22) is performed over a specifiable time interval because it is limited by the disable pulse generator (fig. 4A, ref. 29). As broadly as claimed, if the disable pulse generator 29 prevents the outputs of the UP (25) and DOWN (27) count generators from being updated to the SIN and COS lookup tables, it causes their respective accumulation outputs "UP COUNT" and "DOWN COUNT" to be "specifiable" as claimed. Liessner specifically describes the operation of the disable pulse generator (fig. 4A, ref. 29; ***col.***

4, lines 30-40) as preventing a count from occurring but for a specified time interval determined by the pulse generator.

The Applicant's argument rests upon the insistence that Liessner could not disclose the claimed "accumulation over a specifiable time interval" because no *clock signal* is employed by Liessner. However, the use of a clock signal to determine the specifiable time interval is not whatsoever claimed. Nothing in the present claims require the use of a clock signal to specify the "specifiable time interval" as argued by the Applicant. Nothing in the claims require that the use of a clock signal is inherent, imputed, or implied in the claimed invention. Even if Liessner does teach away from the use of a clock signal, it should have no bearing upon the applicability of Liessner as a prior art reference against the current set of claims.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jason M. Perilla/
Art Unit 2611
August 13, 2009

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